IN THE CLAIMS

Please amend the following claims which are pending in the present application:

What is claimed:

1-18. (Canceled)

19. (Currently amended) A method of assembling a multi-chip device comprising:

providing an interposer having a first surface and a second surface;

populating the second surface of the interposer with a plurality of conductive pads;

coupling solder balls to only preselected conductive pads of the plurality of conductive pads that are intended to be used, the preselected conductive pads being less than all of the plurality of conductive pads;

coupling a plurality of cache memory devices and at least one passive device to the first surface to form a multi-chip subassembly, wherein the at least one passive device is selected from the group consisting of resistors, capacitors, and inductors, some of the plurality of conductive pads not being coupled to either the plurality of memory devices or the at least one passive device;

testing the plurality of cache memory devices and only a portion of those conductive pads that have solder balls attached of the plurality of conductive pads on the interposer;

coupling the interposer to a substrate with the solder balls and coupling a microprocessor device to the substrate after the testing if the plurality of cache memory devices pass the testing; and

not coupling the interposer to the substrate and not coupling the microprocessor device to the ~~interposer~~ substrate if the plurality of cache memory devices does not pass the testing.

20. (Canceled)

21. (Previously Presented) The method of claim 19 wherein the interposer comprises organic material.

22. (Withdrawn) The method of claim 19 wherein coupling at least one semiconductor die comprises a C4 process.

23. (Canceled)

24. (Withdrawn) The method of claim 19 further comprising coupling a single chip carrier to the substrate.

25. (Withdrawn) The method of claim 19 wherein coupling at least one semiconductor die comprises coupling memory chips to the interposer.

26. (Previously presented) The method of claim 19, further comprising:

creating a plurality of contacts on the substrate; and

electrically connecting the preselected conductive pads of the plurality of conductive pads to the plurality of contacts.

REMARKS

Support for Claim Limitations

Listed below, for the Examiner's convenience, are all of the claimed limitations including reference numerals and indications of where support for the limitations can be found in the disclosure.

Claim 19:

- Providing an interposer (12) having a first surface (13) and a second surface (24) – page 7, lines 12-13; page 8, lines 1-2.
- Populating the second surface (24) of the interposer (12) with a plurality of conductive pads (26) – page 8, lines 8-10.
- Coupling solder balls (30) to only preselected conductive pads (26) of the plurality of conductive pads (26) that are intended to be used, the preselected conductive pad (26) being less than all of the plurality of conductive pads – page 9, lines 3-14.
- Coupling a plurality of cache memory devices (16) and at least one passive device (18) to the first surface (13) to form a multi-chip subassembly (10) wherein the at least one passive device (18) is selected from the group consisting of resistors, capacitors, and inductors, not all of the conductive pads (26) being coupled to at least one of the plurality of memory devices (16) and the at least one passive device (18) – page 7, lines 12-15; page 9, lines 5-13.
- Testing the plurality of cache memory devices (16) and only a portion of those conductive pads (26) that have solder balls (30)

attached of the plurality of conductive pads (26) on the interposer (12) – page 9, lines 10-14; page 10, lines 5-9.

- Coupling the interposer (12) to a substrate (50) with the solder balls (30) and coupling a microprocessor device (52) to the substrate (50) after the testing if the plurality of cache memory devices (16) pass the testing – page 10, lines 3-13.
- Not coupling the interposer to the substrate and not coupling the microprocessor device to the substrate if the plurality of cache memory devices does not pass the testing – page 10, lines 8-13.

Claim 21:

- The interposer (12) comprises organic material – page 7, lines 9-10.

Claim 26:

- Creating a plurality of contacts (30) on the substrate (12) – page 5, lines 10-12.
- Electrically connecting the preselected conductive pads (26) of the plurality of conductive pads (26) to the plurality of contacts (30) – page 5, lines 8-12.

Applicant submits that the locations in the specification as filed listed above may not be the only locations in the specification where the respective limitations can be found.

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 19, 21 and 26 under 35 U.S.C. § 103(a) as being unpatentable over Seidel in view of Gedney, and further in view of Beers, Degani, Hamzehdoost, and Mennitt.

Claim 19 includes coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Specifically, claim 19 includes the limitations "populating the second surface of the interposer with a plurality of conductive pads," "coupling solder balls to only preselected conductive pads of the plurality of conductive pads that are intended to be used, the preselected conductive pads being less than all of the plurality of conductive pads," and "some of the plurality of conductive pads not being coupled either the plurality of memory devices or the at least one passive device."

Seidel does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Seidel teaches a device and method for testing the integrity of electrical connectors on a substrate (Abstract). As illustrated in Figures 1 and 2, a ceramic substrate 10 has a plurality of solder balls 12 on one surface thereof and semiconductor chips 11 on an opposing surface thereof (Col. 2, lines 44-48). The testing apparatus 14 has a plurality of pins 16 thereon (Col. 2, lines 52-54). Each of the pins 16 has four electrically conductive strips 18a, 18b, 18c, and 18d which are

circumferentially spaced there around (Col. 2, lines 54-56). Each conductive strip can be used independently for test and/or burn-in signals and power (Col. 2, lines 60-62). Seidel makes no mention of conductive pads on the substrate. Seidel thus teaches a test apparatus having a plurality of pins with conductive strips thereon. Specifically, Seidel does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Gedney does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Gedney teaches a package for mounting integrated circuit chips onto a circuit board (Abstract). As illustrated in Figures 4 and 5, a conventional integrated circuit chip 20 is provided which has an array of input/output pads 22 on one side thereof which provide not only input/output signal connections to and from the chip, but also power and ground connections (Col. 6, lines 36-39). A chip carrier 24 is provided which has a top surface 26 and a bottom surface 28. The top surface 26 of the chip carrier 24 has an array of bonding pads 30 which are arranged in a pattern which corresponds to the pattern or footprints of the I/O pads 22 on the chip 20 (Col. 6, lines 44-52). The bottom surface 28 of the chip carrier 24 has a second set of bonding pads 32 which are connected to the set of bonding pads 30 by metal plated vias 34 (Col. 6, lines 52-55). Since the chip carrier 24 is larger than the chip 20, the spacing between the bonding pads 32 on the bottom surface can be and normally is larger than the spacing between the bonding

pads 30 on the top surface (Col. 6, lines 62-65). The chip 20 is mounted to the chip carrier 24 by means of solder balls 36 which interconnect the I/O pads 22 on the chip 20 to the bonding pads 30 on the top surface of the chip carrier 24 (Col. 7, lines 47-50). Gedney makes no mention of coupling solder balls to only some of the conductive pads, and as illustrated in Figure 5, each conductive pad 22, 30, 32, and 42 has a solder ball connected thereto. Gedney thus teaches interconnecting a (an)?? integrated circuit chip, a chip carrier, and circuit board with conductive pads and solder balls, each conductive pad being connected to a solder ball. Specifically, Gedney does teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Beers does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Beers teaches the use of a conveyor transporting circuit boards through a production line (Abstract). Beers makes absolutely no mention or reference to conductive pads on a substrate of any kind. Specifically, Beers does not teach or suggest coupling coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Degani does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Degani teaches an interconnect strategy for memory chip

packages to reduce or eliminate alpha particle contamination through the use of high lead solder interconnections in the vicinity of semiconductor memory cells (Abstract). As illustrated in Figures 1 and 2, semiconductor chips 12, 13, and 14 are bonded to an interconnection substrate 11 (Col. 3, lines 16-18). Bonding pads on the interconnect substrate are shown at 15, bonding pads on the chips are shown at 16, and solder bump pillars are shown at 17 (Col. 3, lines 43-46). The bonding pads 16 on the semiconductor chip are typically aluminum and are coated with under bump metallization to impart solder ability. The pads 16 shown on the substrate are typically part of a printed circuit. The solder pillars 17 are typically formed from solder bumps (Col. 3, lines 46-53). Degani makes no mention of connecting solder balls to only some of the contact pads, and as illustrated in Figure 2, the semiconductor chips and the substrate are interconnected by conductive pads and solder balls, with each contact pad having a solder ball attached thereto. Specifically, Degani does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Hamzehdoost does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Hamzehdoost teaches a multi-layer substrate structure and a method for fabricating the same (Abstract). As illustrated in Figure 3a, holes 26a, and 26b, and epoxy layers 24a, and 24b, are plated with a conductive metal layer 30 (Col. 3, lines 40-42). This new conductive metal layer 30 is then patterned

and etched as is desired (Col. 3, lines 42-43). Next, a solder mask 32 is applied, preferably using a screen printing or photo imaging procedure known in the art (Col. 3, lines 43-45). During such procedure, the entire exposed surfaces of the conductive metal layer 30 is covered with a compatible material, except for selective wire bondable areas 34 and for selective solder ball areas 36 where it is desired to have the solder balls applied (Col. 3, lines 46-50). As illustrated in Figure 3d, a semiconductor integrated circuit die 38 is connected to a central region of the substrate (Col. 3, lines 52-53). A plurality of solder balls 44, as illustrated in Figure 4, are (is??) attached to the elective solderable areas 36 in order to form the completed integrated circuit chip package 110 (Col. 3, lines 61-63). As clearly illustrated in Figure 4, each selective solderable area 36 has a solder ball 44 attached thereto. Hamzehdoost thus teaches forming a plurality of solderable areas on a substrate and attaching a solder ball to each solderable area. Specifically, Hamzehdoost does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Mennitt does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate. Mennitt teaches a semiconductor device that has test-only contacts to reduce the size of the device and eliminate unnecessary external contacts (Abstract). As illustrated in Figure 5, test pads 32 are provided on the top surface of the package substrate 12 whereas solder balls are attached to the bottom surface (Col. 7, lines 40-42). Test pads 32 may be formed on the bottom of the package

substrate 12 as well, as illustrated in Figure 6 (Col. 7, lines 46-48). Both the solder balls 26 and test pads 32 can be contacted during testing with conventional testing equipment (Col. 7, lines 50-54). Therefore the test pads 32 are for testing the integrated circuit on the package substrate 12 and are coupled to such a device. Mennitt thus teaches conductive pads on a package substrate coupled to a device on the package substrate to test the device. Specifically, Mennitt does not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Specifically, Seidel, Gedney, Beers, Degani, Hamzehdoost, and Mennitt do not teach or suggest coupling solder balls to only some of a plurality of conductive pads on a substrate where not all of the pads are coupled to a device on the substrate.

Therefore, claim 19 is patentable over Seidel in view of Gedney, and further in view of Beers, Degani, Hamzehdoost, and Mennitt because claim 19 includes a limitation that is not taught or suggested by Seidel, Gedney, Beers, Degani, Hamzehdoost, and Mennitt.

Claims 21 and 26 are dependent claim 19 and should be allowable for the same reasons as claim 19 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 19, 21, and 26 under 35 U.S.C. § 103(a) as being unpatentable over Seidel in view of Gedney, and further in view of Beers, Degani, Hamzehdoost, and Mennitt.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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